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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,194	03/22/2004	Yoshihisa Shimazu	60188-811	1135

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EXAMINER	
MOREHEAD, JOHN H	

ART UNIT	PAPER NUMBER
2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/805,194	SHIMAZU ET AL.	
	Examiner	Art Unit	
	John Morehead	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-5 and 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki US 7,116,358, in view of Nagasaki et al US 5,153,730.

5. Re claim 1, Sasaki discloses an image processing device (fig. 1) for performing image processing for an image signal output from an image sensor and outputting the results (col. 15 lines 30-53), comprising: an internal memory having line memories (fig. 14 and fig. 25 elements 61a and 61b, elements 92a through 92d, it is noted that the line memories are located in the real time processing unit element 23) for storing an image

by row or column as a unit (column 38 lines 63-65, shows that the pixels are stored in the line memory horizontally, i.e. row); an image processing section (fig. 1 element 23) for performing the image processing using the internal memory (line memory is located within real time processing unit); and a CPU (fig. 1 element 24) for controlling the image processing section (col. 15 lines 58-64 also), wherein the image processing section includes a plurality of processing circuits (fig. 3 element 23) each performing predetermined processing as the image processing (col. 16 lines 43-52, also external memory will be considered element 29).

Sasaki fails to disclose the CPU determines whether or not each predetermined processing is performed with use of an external memory. However, Nagasaki discloses an electronic still camera which contains a control section (CPU) that controls various circuits for processing signals, furthermore it allows the processed signal to be sent to different memory allocations (Nagasaki, col. 5 lines 39-43, col. 7 lines 3-15 and 22-46).

Therefore taking the combined teachings of Sasaki and Nagasaki, as a whole, it would have been obvious to one of ordinary skill in the art to modify Sasaki's image processing device to incorporate Nagasaki's control section (CPU) to be able to send different image processing devices to different memory allocation units either internally or externally via the CPU.

Re claim 2, the combined teachings of Sasaki and Nagasaki, as a whole, further discloses the device of Claim 1, the image processing section performs given processing as the image processing without use of the external memory when the given

processing can be performed without use of the external memory (Sasaki, col. 15 lines 58-64).

Re claim 3, the combined teachings of Sasaki and Nagasaki, as a whole, further discloses the device of Claim 1, wherein the CPU outputs a control signal for reducing power consumed by the external memory when the image processing section does not use the external memory (the above limitation is not explicitly stated by Sasaki, however it is inherent that if the external memory is not being used, then the apparatus is consuming less power).

Re claim 4, the combined teachings of Sasaki and Nagasaki, as a whole, further discloses the device of Claim 1, wherein the image processing section includes as the plurality of processing circuits: a luminance/color-difference signal processing circuit (Sasaki, fig. 3 element 42) for converting the image signal obtained from the image sensor to a luminance signal and a color-difference signal and outputting the converted signals (Sasaki, col. 22 lines 16-47); and a compression circuit (Sasaki, fig. 1 element 31) for performing compression coding of an image corresponding to the output of the luminance/color-difference signal processing circuit and outputting the results as an output of the image processing section (Sasaki, col. 16 lines 13-20).

Re claim 5, the combined teachings of Sasaki and Nagasaki, as a whole, further discloses the device of Claim 1, wherein the image processing section includes an on-

screen display processing circuit (Sasaki, fig. 1 element 27c) for superimposing an image read from the external memory on the image obtained from the image sensor and outputting the results (Sasaki, fig. 1, col. 16, the display module element 27c and the main memory element 29 are connected to the same bus, therefore an image can be read from the external memory and the results outputted on the LCD element 27).

Re claim 7, the combined teachings of Sasaki and Nagasaki, as a whole, further discloses the device of Claim 1, wherein at least two of the plurality of processing circuits perform processing using the same internal memory (Sasaki, fig. 25 col. 35 lines 26-35).

Re claim 8, the combined teachings of Sasaki and Nagasaki, as a whole, further discloses the device of Claim 1, wherein the image processing section stores the image output from the image sensor into the external memory, reads the stored image from the external memory by row or column as a unit whichever has a smaller number of pixels, performs the image processing for the read data using the internal memory, stores the results into an area of the external memory in which the corresponding pixel data had been stored before being read, and reads the resultant image from the external memory to be output (Sasaki, col. 38 lines 66-67, col. 39 lines 1-35, once the horizontal pixels exceed the number of line memories, the image is stored temporarily in the main memory and that image is horizontally divided into multiple blocks and then image processing is done on the multiple blocks by the real time processing unit).

Re claim 9, the combined teachings of Sasaki and Nagasaki, as a whole, further discloses the device of Claim 8, wherein the image processing section divides the image into a plurality of areas if the number of pixels of each row or column of the image whichever is smaller exceeds the number of pixels allowed to be stored in the internal memory (Sasaki, col. 38 lines 63-67 and col. 39 lines 1-35).

Re claim 10, the combined teachings of Sasaki and Nagasaki, as a whole, further discloses a camera comprising: the image processing device of Claim 4; an image sensor for outputting an image signal to the image processing device; and a recording device (Sasaki, fig. 1 element 30) for writing an output of the image processing device into a recording medium (Sasaki, col. 15 lines 51-53).

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki US 7116358 in view of Nagasaki '730 and in view of Wakeland US 5966116.

Re claim 6, claim 6 further requires the device of Claim 1, wherein one of the plurality of processing circuits stores a processed image into the external memory sequentially by row or column as a unit, and another one of the plurality of processing circuits reads the image stored in the external memory by column or row as a unit whichever different from the unit used during the storing of the image.

Sasaki fails to disclose the above teachings as recited in claim 6, however Wakeland teaches a hardware rotation unit that rotates a portrait image 90 degrees in a

clockwise or counter-clockwise direction in order to create a landscape image (Wakeland, fig. 5, col. 10 lines 35-50).

Therefore taking the combined teachings of Sasaki and Wakeland, as a whole, it would have been obvious to one of ordinary skill in the art to combine Sasaki's image processing circuit with Wakeland's hardware rotation unit by connecting the hardware rotation unit to the main bus of Sasaki's image processing circuit so that the LCD screen can see images in either portrait or landscape views.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Morehead whose telephone number is 571-270-1183. The examiner can normally be reached on Monday - Friday (alt) 7:30-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ngoc Yen Vu can be reached on 571-272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JHM 12/21/2007

NGOC-YEN VU
SUPERVISORY PATENT EXAMINER